Notice of Allowability	Application No.	Applicant(s)	
	09/838,395	CALVIGNAC ET AL.	
	Examiner	Art Unit	
	John Pezzlo	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed 19 April 2001*.

2. ☒ The allowed claim(s) is/are *1-9*.

3. ☒ The drawings filed on *19 April 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6 August 2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JOHN PEZZLO
PRIMARY EXAMINER

DETAILED ACTION

Allowable Subject Matter

Claims 1-9 are allowable over the prior art of record.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: Applicants have claimed the following uniquely distinct features in the instant invention, which are not found in the prior art, either singularly or in combination.

1. Regarding claim 1 – A device including: a Network Processor Complex Chip including a plurality of co-processors executing programs that forward frames or hardware assist functions that performs operations like table searches, policing and counting, a Data Flow Chip operatively coupled to the Network Processor Complex Chip, said Data Flow Chip including at least one port to receive/transmit data and circuit arrangement that sets the at least one port into switch mode and/or line mode, and a Scheduler Chip operatively coupled to the Data Flow Chip, said Scheduler Chip scheduling frames to meet predetermined Quality of Service commitments.

2. Regarding claim 3 – A device including: an ingress section and an egress section symmetrically arranged, said ingress section and said egress section each including Network Processor Complex Chip having a plurality of co-processors programmed to

execute code that forwards network traffic, a Data Flow Chip operatively coupled to the Network Processor Complex Chip, said Data Flow Chip having at least one port and circuitry to configure said port into a switch mode or a line mode, and a Scheduler Chip operatively coupled to said Data Flow Chip, said Scheduler Chip including circuits that schedule frames to meet predetermined Quality of Service commitments.

3. Regarding claim 4 – A device including: an ingress section, an egress section symmetrically arranged to said ingress section wherein said ingress section includes a First Data Flow Chip having at least a first input port and a first output port, a First Network Processor Complex Chip operatively coupled to said Data Flow Chip, a First Scheduler Chip operatively coupled to said Data Flow Chip, and said egress section including a second Data Flow Chip having at least a second output and a second input, a second Network Processor Chip operatively coupled to said Second Data Flow Chip, a second Scheduler Chip operatively coupled to the Second Data Flow Chip, and communication media that wraps the Second Data Flow Chip to the First Data Flow Chip.

4. Regarding claim 7 – A device including: an ingress section, and an egress section symmetrically arranged to said ingress section wherein said ingress section includes a First Data Flow Chip having at least a first input port and a first Output port; a First Network Processor Chip operatively coupled to said Data Flow Chip, a First Scheduler Chip operatively coupled to said Data Flow Chip, and said egress section including a second Data Flow Chip having at least a second Output port and a second input port, a

second Network Processor Chip operatively coupled to said Second Data Flow Chip, a second Scheduler Chip operatively coupled to the Second Data Flow Chip, communication media that wraps the Second Data Flow Chip to the First Data Flow Chip, a first interface operatively coupled to the first output port and the second input port, and a second interface operatively coupling the first input port and the second output Port.

5. Regarding claim 8 – A network device including: a switch fabric and a plurality of Network Processors connected in parallel to said switch fabric wherein each of the Network Processors including an ingress section, an egress section symmetrically arranged to said ingress section wherein said ingress section including a First Data Flow Chip having at least a first input port and a first output port; a First Network Processor Complex Chip operatively coupled to said first Data Flow Chip, a First Scheduler Chip operatively coupled to said Data Flow Chip, and said egress section including a second Data Flow Chip having at least a second output port and a second input port a second Network Processor Chip operatively coupled to said Second Data Flow Chip, a second Scheduler Chip operatively coupled to the Second Data Flow Chip, communication media that wraps the Second Data Flow Chip to the First Data Flow Chip, a first interface operatively coupled to the first output port and the second input port and a second interface operatively coupling the first input port and the second output port.

6. Regarding claim 9 – A Network Processor including: a Network Processor Complex Chip having a plurality of co-processors, a memory operatively connected to

said Network Processor, and a Data Flow Chip operatively coupled to said Network Processor Chip, said Data Flow Chip including at least an output port, an input port, and control mechanism that sets at least the input port or the output port into a switch mode or a line mode.

The closest prior art either singularly or in combination, fail to anticipate or render the above limitations obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Claims 1-9 being allowable, **Prosecution On The Merits Is Closed** in this application.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Barker et al. (US 6,766,381 B1) discloses a VLSI network processor and methods.

2. Wilford et al. (US 6,687,247 B1) discloses an architecture for high speed class of service enabled linecard.

3. Viswanadham et al. (^,424,659 B2) discloses a multi-layer switching apparatus and method.

4. Tirabassi et al. (US 6,400,925 B1) discloses a packet switch control with layered software.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Pezzlo whose telephone number is (571) 272-3090. The examiner can normally be reached on Monday to Friday from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C.

or faxed to:

(703) 872-9306

For informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand delivered responses should be brought to:

Jefferson Building

500 Dulany Street

Alexandria, VA.

John Pezzlo

18 February 2005

JOHN PEZZLO
PRIMARY EXAMINER